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10/727,850	12/03/2003	Steven Perry	ALTRP106/A1237	7931

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EXAMINER	
FENNEMA, ROBERT E	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/727,850	PERRY, STEVEN	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 are pending. Claims 1, 5, 11, 14, 19, and 27 have been amended as per Applicants request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 19-20, and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Owen et al. (USPN 4,876,660, herein Owen). Claims 1, 19, and 27 have been interpreted two different ways in light of the amendment, both interpretations and rejections have been listed below.

4. As per Claim 1, Owen teaches: A processor, comprising:

a plurality of registers (Column 8, Lines 24-26, Accumulators 40 and 42. Also see Column 9, Lines 19-20), wherein each of the plurality of registers is a processor register and comprises data bits for holding data and one or more flag and status bits for holding carry flag information (Column 4, Lines 27-31 and Column 9, Lines 33-34 and 40 disclose the flag and status bits, while Column 9, Lines 29-34 disclose that the register is holding the data and the status bits/flags);

an arithmetic logic unit (Figure 6a, Adder 34, also see Column 9, Lines 38-41), the arithmetic logic unit coupled to the plurality of registers, wherein the arithmetic logic unit is operable to read and write data and carry flag information to one of the plurality of registers (Column 9, Lines 38-47, and Column 8, Lines 28-30, which states the data can be written into either one or both of the registers, while Figure 6a shows the adder can read the registers through MUX 54).

5. As per Claim 1, Owen teaches: A processor, comprising:

a plurality of registers (Column 8, Lines 24-26, Accumulators 40 and 42. Also see Column 9, Lines 19-20), wherein each of the plurality of registers is a processor register and comprises data bits for holding data and one or more flag and status bits for holding carry flag information (Column 4, Lines 27-31 and Column 9, Lines 33-34 and 40 disclose the flag and status bits, while Column 9, Lines 29-34 disclose that the register is holding the data and the status bits/flags);

an arithmetic logic unit (Figure 6a, Adder 34, also see Column 9, Lines 38-41, in combination with MUX 62. These two objects together provide equivalent functionality as what is claimed, where MUX 62 can read the registers, while the adder reads and writes, as a unit is not necessarily a single object), the arithmetic logic unit coupled to the plurality of registers, wherein the arithmetic logic unit is operable to read and write data and carry flag information to one of the plurality of registers (Column 9, Lines 38-47, and Column 8, Lines 28-30, which states the data can be written into either one or both of the registers).

6. As per Claim 2, Owen teaches: The processor of claim 1, wherein the one or more flag and status bits hold overflow flag information (Column 4, Lines 27-31, and Column 9, Lines 36-37).

7. As per Claim 19, Owen teaches: A method of processing data, comprising:

providing data to an arithmetic logic unit (Figure 6a, Adder 34, also see Column 9, Lines 38-41) associated with a processor, the data obtained from registers (Column 8, Lines 30-40, which disclose how the registers feedback into the adder) comprising data bits for holding data and one or more flag and status bits for holding carry flag information (Column 4, Lines 27-31 and Column 9, Lines 33-34 and 40 disclose the flag and status bits, while Column 9, Lines 29-34 disclose that registers (Accumulator 40 or 42) are holding the data and the status bits/flags);

processing the data at the arithmetic logic unit (Column 9, Lines 38-43), the arithmetic logic init coupled a the plurality of registers including a processor register, wherein the arithmetic logic unit is operable to read and write data and carry flag information to the processor register (Column 9, Lines 38-47, and Column 8, Lines 28-30, which states the data can be written into either one or both of the registers, while Figure 6a shows the adder can read the registers through MUX 54).

8. As per Claim 19, Owen teaches: A method of processing data, comprising:

providing data to an arithmetic logic unit (Figure 6a, Adder 34, also see Column 9, Lines 38-41) associated with a processor, the data obtained from registers (Column 8, Lines 30-40, which disclose how the registers feedback into the adder) comprising data bits for holding data and one or more flag and status bits for holding carry flag information (Column 4, Lines 27-31 and Column 9, Lines 33-34 and 40 disclose the flag and status bits, while Column 9, Lines 29-34 disclose that registers (Accumulator 40 or 42) are holding the data and the status bits/flags);

processing the data at the arithmetic logic unit (Figure 6a, Adder 34, also see Column 9, Lines 38-43, in combination with MUX 62. These two objects together provide equivalent functionality as what is claimed, where MUX 62 can read the registers, while the adder reads and writes, as a unit is not necessarily a single object), the arithmetic logic init coupled a the plurality of registers including a processor register, wherein the arithmetic logic unit is operable to read and write data and carry flag information to the processor register (Column 9, Lines 38-47, and Column 8, Lines 28-30, which states the data can be written into either one or both of the registers).

9. As per Claim 20, Owen teaches: The method of claim 19, wherein the one or more flag and status bits hold overflow flag information (Column 4, Lines 27-31, and Column 9, Lines 36-37).

10. As per Claim 27, Owen teaches: A programmable chip, comprising:

means for providing data to an arithmetic logic unit associated with a processor on the programmable chip (Column 8, Lines 30-40, which disclose how the registers feedback into the adder), the data obtained from registers comprising data bits for holding data and one or more flag and status bits for holding carry flag information (Column 4, Lines 27-31 and Column 9, Lines 33-34 and 40 disclose the flag and status bits, while Column 9, Lines 29-34 disclose that the register is holding the data and the status bits/flags);

means for processing the data at the arithmetic logic unit (Column 9, Lines 38-43), the arithmetic logic unit coupled to a plurality of registers including a processor register, where the arithmetic logic unit is operable to read and write data and carry flag information to the processor register (Column 9, Lines 38-47, and Column 8, Lines 28-30, which states the data can be written into either one or both of the registers, while Figure 6a shows the adder can read the registers through MUX 54).

11. As per Claim 27, Owen teaches: A programmable chip, comprising:

means for providing data to an arithmetic logic unit associated with a processor on the programmable chip (Column 8, Lines 30-40, which disclose how the registers feedback into the adder), the data obtained from registers comprising data bits for holding data and one or more flag and status bits for holding carry flag information (Column 4, Lines 27-31 and Column 9, Lines 33-34 and 40 disclose the flag and status bits, while Column 9, Lines 29-34 disclose that the register is holding the data and the status bits/flags);

means for processing the data at the arithmetic logic unit (Figure 6a, Adder 34, also see Column 9, Lines 38-43, in combination with MUX 62. These two objects together provide equivalent functionality as what is claimed, where MUX 62 can read the registers, while the adder reads and writes, as a unit is not necessarily a single object), the arithmetic logic unit coupled to a plurality of registers including a processor register, where the arithmetic logic unit is operable to read and write data and carry flag information to the processor register (Column 9, Lines 38-47, and Column 8, Lines 28-30, which states the data can be written into either one or both of the registers).

12. As per Claim 28, Owen teaches: The programmable chip of claim 27, wherein the one or more flag and status bits hold overflow flag information (Column 4, Lines 27-31, and Column 9, Lines 36-37).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 3, 21, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen, in view of Baldwin (USPN 5,042,000, herein Baldwin).

15. As per Claim 3, Owen teaches the processor of claim 2, but fails to explicitly teach: wherein the one or more flag bits hold sticky overflow flag information. Owen teaches an overflow bit, but does not specify whether it is a "sticky" overflow bit or not. Baldwin teaches that a "sticky" status bit may be used in situations where it is preferable to monitor fault conditions separately from the primary error-handling mechanism (Column 95, Lines 50-64). The advantage of this, as Baldwin discloses, is being able to see and operate on the flag after a series of operations, instead of checking at each individual operation. Given these advantages, one of ordinary skill in the art at the time the invention was made would have implemented Baldwin's "sticky" overflow bit into Owens invention if they wanted to bypass the normal error-handling mechanisms for certain series of instructions.

16. As per Claim 21, Owen teaches the method of claim 20, but fails to explicitly teach: wherein the one or more flag bits hold sticky overflow flag information. Owen teaches an overflow bit, but does not specify whether it is a "sticky" overflow bit or not. Baldwin teaches that a "sticky" status bit may be used in situations where it is preferable to monitor fault conditions separately from the primary error-handling mechanism (Column 95, Lines 50-64). The advantage of this, as Baldwin discloses, is being able to see and operate on the flag after a series of operations, instead of checking at each individual operation. Given these advantages, one of ordinary skill in the art at the time the invention was made would have implemented Baldwin's "sticky" overflow bit into

Owens invention if they wanted to bypass the normal error-handling mechanisms for certain series of instructions.

17. As per Claim 29, Owen teaches the programmable chip of claim 28, but fails to explicitly teach: wherein the one or more flag bits hold sticky overflow flag information. Owen teaches an overflow bit, but does not specify whether it is a "sticky" overflow bit or not. Baldwin teaches that a "sticky" status bit may be used in situations where it is preferable to monitor fault conditions separately from the primary error-handling mechanism (Column 95, Lines 50-64). The advantage of this, as Baldwin discloses, is being able to see and operate on the flag after a series of operations, instead of checking at each individual operation. Given these advantages, one of ordinary skill in the art at the time the invention was made would have implemented Baldwin's "sticky" overflow bit into Owens invention if they wanted to bypass the normal error-handling mechanisms for certain series of instructions.

18. Claims 4-14,18, 21, 22-26, and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen, in view of Parady (USPN 5,933,627).

19. As per Claim 4, Owen teaches the processor of claim 1, but fails to explicitly teach: wherein the processor is a multithreaded processor.

Owen teaches a processor, namely a multiplier-accumulator unit and the supporting hardware to execute arithmetic operations, but does not teach about the

overall system it could be implemented on. Parady teaches a multithreaded microprocessor (Parady Column 2 Lines 18-20) which interleaves threads on a cycle-by-cycle basis in round robin fashion (Column 3, Lines 18-19, and Column 2, Lines 6-8, which state that fine-grained processors interleave on a cycle-by-cycle basis, Column 2, Lines 32-34, and Column 4, Lines 9-10, the embodiment in which round-robin is used). Owen teaches that the advantage of his system is higher density, which leads to fewer parts, lower power requirements, and increases system speed due to interconnection delay being reduced (Column 3, Lines 32-40). Given these advantages, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the multiplier-accumulator circuit of Owens design into the multithreaded system of Parady's, to enhance the speed and decrease the power consumption of Parady's system.

20. As per Claim 5, Parady teaches: The processor of claim 1, wherein providing flag and status information in each of the plurality of registers allows the processor to handle a plurality of threads, wherein each thread uses disparate flag and status bits (Column 1, Lines 17-20. In a multi-threaded environment, each thread is working on a different part of the program, and would therefore be not be writing the same flag and status bits).

21. As per Claim 6, Parady teaches: The processor of claim 5, wherein the plurality of threads are each associated with a subset of the plurality of registers (Column 2, Lines 35-36).

22. As per Claim 7, Parady teaches: The processor of claim 6, further comprising context circuitry associated with the plurality of threads, wherein the context circuitry is operable to track which of the plurality of threads is being processed by a particular stage (Column 3, Line 57 – Column 4, Line 30).

23. As per Claim 8, Parady teaches: The processor of claim 7, wherein the arithmetic logic unit is operable to process the plurality of threads, the arithmetic logic unit configured to process a particular thread for a single clock cycle before context switching to process a next thread, wherein each of the plurality of threads are processed for the single clock cycle before context switching (Column 4, Lines 9-10).

24. As per Claim 9, Parady teaches: The processor of claim 1, wherein the processor is a processor core on a programmable chip (Column 1, Lines 11-12).

25. As per Claim 10, Parady teaches: The processor of claim 8, wherein the particular thread is processed for a single clock cycle to allow a memory access to complete before continuing processing of the particular thread (Column 4, Lines 42-48).

26. As per Claim 11, Parady teaches: The processor of claim 10, further comprising a plurality of program counters, where the program counters track the processing location of each thread (Column 3, Lines 50-55).

27. As per Claim 12, Parady teaches: The processor of claim 1, wherein the plurality of registers are configured as memory (Column 2, Lines 25-26) on a programmable chip (Column 1, Lines 11-12).

28. As per Claim 13, Parady teaches: The processor of claim 1, wherein the processor is a central processing unit or a digital signal processor (Figures 1 and 2, the Ultrasparc processor, where a CPU is defined by the Dictionary of Computers, Information Processing & Telecommunications as "a unit of a computer that includes circuits controlling the interpretation and execution of instructions).

29. As per Claim 14, Parady teaches: The processor of claim 1, wherein context circuitry is a context register (Column 4, Lines 9-12).

30. As per Claim 18, Parady teaches: The processor of claim 10, further comprising a plurality of program counters associated with the plurality of threads (Column 2, Lines 25-32, the program address registers).

31. As per Claim 22, Owen teaches the method of claim 19, but fails to explicitly teach: wherein the processor is a multithreaded processor.

Owen teaches a processor, namely a multiplier-accumulator unit and the supporting hardware to execute arithmetic operations, but does not teach about the overall system it could be implemented on. Parady teaches a multithreaded microprocessor (Parady Column 2 Lines 18-20) which interleaves threads on a cycle-by-cycle basis in round robin fashion (Column 3, Lines 18-19, and Column 2, Lines 6-8, which state that fine-grained processors interleave on a cycle-by-cycle basis, Column 2, Lines 32-34, and Column 4, Lines 9-10, the embodiment in which round-robin is used). Owen teaches that the advantage of his system is higher density, which leads to fewer parts, lower power requirements, and increases system speed due to interconnection delay being reduced (Column 3, Lines 32-40). Given these advantages, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the multiplier-accumulator circuit of Owens design into the multithreaded system of Parady's, to enhance the speed and decrease the power consumption of Parady's system.

32. As per Claim 23, Parady teaches: The method of claim 19, where providing flag and status information in each of the plurality of registers allows the processor to handle a plurality of threads, wherein each thread uses writes disparate flag and status bits (Column 1, Lines 17-20. In a multi-threaded environment, each thread is working on a

different part of the program, and would therefore be not be writing the same flag and status bits).

33. As per Claim 24, Parady teaches: The method of claim 23, wherein the plurality of threads are each associated with a subset of the plurality of registers (Column 2, Lines 35-36).

34. As per Claim 25, Parady teaches: The method of claim 24, further comprising context circuitry associated with the plurality of threads (Column 2, Lines 25-32, the program address registers), wherein the context circuitry is operable to track which of the plurality of threads is being processed by a particular stage (Column 3, Line 57 – Column 4, Line 30).

35. As per Claim 26, Parady teaches: The method of claim 25, wherein the arithmetic logic unit is operable to process the plurality of threads, the arithmetic logic unit configured to process a particular thread for a single clock cycle before context switching to process a next thread, wherein each of the plurality of threads are processed for the single clock cycle before context switching (Column 4, Lines 42-48).

36. As per Claim 30, Owen teaches the programmable chip of claim 27, but fails to explicitly teach: wherein the processor is a multithreaded processor.

Owen teaches a processor, namely a multiplier-accumulator unit and the supporting hardware to execute arithmetic operations, but does not teach about the overall system it could be implemented on. Parady teaches a multithreaded microprocessor (Parady Column 2 Lines 18-20) which interleaves threads on a cycle-by-cycle basis in round robin fashion (Column 3, Lines 18-19, and Column 2, Lines 6-8, which state that fine-grained processors interleave on a cycle-by-cycle basis, Column 2, Lines 32-34, and Column 4, Lines 9-10, the embodiment in which round-robin is used). Owen teaches that the advantage of his system is higher density, which leads to fewer parts, lower power requirements, and increases system speed due to interconnection delay being reduced (Column 3, Lines 32-40). Given these advantages, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the multiplier-accumulator circuit of Owens design into the multithreaded system of Parady's, to enhance the speed and decrease the power consumption of Parady's system.

37. As per Claim 31, Parady teaches: The programmable chip of claim 27, wherein providing flag and status information in each of the plurality of registers allows the processor to handle a plurality of threads, wherein each thread uses writes disparate flag and status bits (Column 1, Lines 17-20. In a multi-threaded environment, each thread is working on a different part of the program, and would therefore be not be writing the same flag and status bits).

38. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Owen and Parady, further in view of Patterson et al. (herein Patterson).

39. As per Claim 15, Parady teaches: The processor of claim 14, where in the processor comprises a plurality of stages (Figure 1), each stage having an associated context register.

Patterson teaches that in a pipelined processor, pipeline registers must be used to save the data (or context) of each stage, to be able to be passed on to the next stage in the pipeline (A-9). This is an essential part of a pipelined processor to ensure that different stages of the pipeline do not interfere with each other (A-8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include registers in each pipeline stage to maintain the context of the stage for the next stage.

40. As per Claim 16, Parady teaches: The processor of claim 15, wherein each thread is associated with a program counter (Column 2, Lines 25-32, the program address registers).

41. As per Claim 17, Parady teaches: The processor of claim 17, wherein the plurality of stages comprise reading the context register (Column 4, Lines 9-12, a thread has to be selected to run each clock cycle, requiring the register to be read to select one), accessing the program counter (Column 3, Lines 50-56), obtaining an instruction

(Figure 1, Prefetch unit 16, also see Column 3, Lines 2-7), decoding the instruction (Figure 1, Decode unit 14), executing the operation (Column 3, Lines 18-19, the ALUs comprise an execution unit seen in Figures 1 and 3), and writing a result to one of the plurality of registers (Figures 1 and 3, where the output of the ALU (execution unit) is directly connected to the register file).

Response to Arguments

42. Applicant's arguments filed 6/26/2006 have been fully considered but they are not persuasive.

Applicant has argued that adder 34 is Owen is not an arithmetic logic unit, and that an arithmetic logic unit is operable to perform multiple functions, including shifts, logic operations, addition, and subtraction. However, these limitations are not in the claim, and Examiner has given the term "arithmetic logic unit" its broadest reasonable interpretation, which is a logic unit which performs arithmetic. It is inherent that an adder is comprised of logic, and it is a unit. Addition is an arithmetic function, thus, the adder is an arithmetic logic unit in the broadest reasonable sense.

Secondly, applicant has amended the independent claims to change the plurality of registers to "processor" registers. The accumulator registers used by Owen are processor registers, as they are registers that are in a processor. Any register in a processor is a processor register. Furthermore, Applicant has argued that the accumulator registers only allow writes by the adder, and not both reads and writes of carry flag and data information. Examiner refers to wire 50 in Figure 6a, which goes into

MUX 54, MUX 56, and back into the adder. Thus, the adder is operable to read and write data and carry flag information to one of the registers. Applicant may point out that the adder reads just the data from the register, and not the carry information, and the Examiner will use an analogy to illustrate how Owen reads on the claim language of "operable to read and write data and carry flag information". This phraseology is similar to someone stating that they plan to "eat and drink cookies and milk". They do not intend to eat the milk and drink the cookies, but the combination of eating and drinking accomplish the goal of consuming the combination of the milk and the cookies, in the same way that the combination of reading and writing done by Owens adder covers the combination of the data and carry flag information. This is in contrast to language that might state that the unit is operable to read both data and carry flag information, and write both data and carry flag information.

Furthermore, in response to the amendment and change of scope, Examiner has presented an alternate interpretation of Owen, in which the "arithmetic logic unit" is considered to be more than simply the adder, which can be read in more detail above.

Conclusion

43. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert E Fennema
Examiner
Art Unit 2183

RF

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100